VIPERLAB

FULLY CONNECTED **VI**RTUAL AND **P**HYSICAL P**ER**OVSKITE PHOTOVOLTAICS **LAB**

D 10.1

DEFINITION OF KEY DEVICE ARCHITECTURES FOR PEROVSKITE PHOTOVOLTAICS

DELIVERABLE

REPORT

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FULLY CONNECTED VIRTUAL AND PHYSICAL PEROVSKITE PHOTOVOLTAICS LAB VIPERLAB

DELIVERABLE

D 10.1 DEFINITION OF KEY DEVICE ARCHITECTURES FOR PEROVSKITE PHOTOVOLTAICS

Project References

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DISCLAIMER

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1. EXECUTIVE SUMMARY

VIPERLAB is an infrastructure project that aims to create a European environment, where various physical and virtual infrastructures from 13 VIPERLAB partners can be accessed by different users from Europe and abroad. VIPERLAB identifies perovskite PV as the key emerging technology that will be the lever for a future market penetration of EU-based PV production with lowest costs and lowest carbon footprint.

The overall goal of the work package 10 is to provide guidance for the infrastructure and technology development within VIPERLAB by evaluating and optimizing the environmental, social and economic impact of new perovskite-based technologies. To this end, this work package will:

• Provide the data (material, process flows etc.) necessary for such an evaluation
• Evaluate the environmental (Life Cycle Assessment, LCA), social and economic (Levelized Cost of Electricity, LCOE) impact of new perovskite-based technologies and how this impact is affected by the application, device design, choice of equipment and process.

2. INTRODUCTION TO DEVICES OF INTEREST

Perovskite solar cells already are at the edge of breaking the PCE (Power Conversion Efficiency) record of conventional silicon solar cell. In the first project period of VIPERLAB, four key architectures of Perovskite solar cells (PSCs) are defined for selection. Depending on whether the electron transport layer (ETL) or the hole transport layer (HTL) is deposited first, the PSC can be manufactured to the so-called "standard architecture" (negative-intrinsic-positive, NIP-type) or "inverted architecture" (positive-intrinsic-negative, PIN-type), respectively Figure 1.

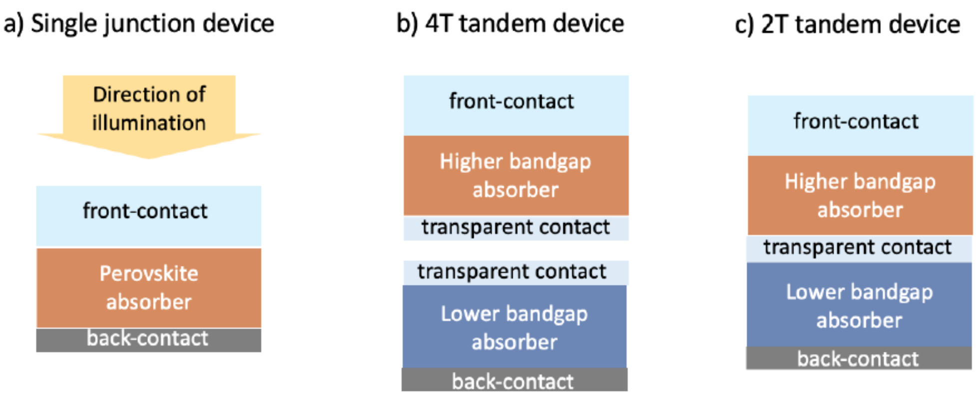

Figure 1 Selected key device architectures for VIPERLAB project (Source: Eva Unger, HZB).

Furthermore, the 2-terminal (2T) and 4-terminal (4T) tandem architectures have a theoretical efficiency limit of up to 43% (Lemercier et al. 2020). The tandem PSCs produce between 98% and 103% of the estimated energy yield (EY) based on the location. This gives good assurance that tandem cells can deliver considerably boosted EYs under real world conditions. Despite slightly better efficiencies for the semi-transparent NIP-type devices, the semi-transparent PIN-type counterparts also appear to be optically attractive for (two-terminal) tandem applications (Lemercier et al. 2020). PSC tandem devices have achieved efficiencies of 29.2% (Emiliano Bellini 2021) and

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29.8% HZB 2021) for 4T and 2T architectures, respectively. Therefore, the 2T (Figure 1c) and 4T (Figure 1b) tandem architectures are also reviewed as potential architectures for manufacturing.

2.1. POSITIVE-INTRINSIC-NEGATIVE (PIN)

In a planar PIN perovskite architecture, at first the HTM layer is deposited and subsequently, the ETM layer. The first planar hetero-junction PSC with a PIN structure was developed in 2015 (Wei et al. 2015) after it was found that perovskites are capable of transporting the holes themselves in 2014. With this advancement, the PIN architecture has expanded the options to explore more for selective layer from organic to inorganic materials and the use of oxide HTM allow for constructing mesoscopic PIN device architecture (Zuo et al. 2016). The highest efficiencies reported in the literature are indeed for planar PIN PCSs (22.3%) (Zheng et al. 2020).

Planar PIN PSC offers low-temperature processing, negligible hysteresis behaviour. Such an architecture has the possibility of eliminating the need of dopants in the HTL and has compatibility with organic electronics manufacturing processes. (Zuo et al. 2016)

The PIN PSCs allow the reduction of parasitic absorption in the front metal contact, as compared to the standard architecture (Lemercier et al. 2020). PIN PSC can systematically include fullerene materials as ETLs because of their good affinity with perovskites as a passivating layer. But they are also known to have a large parasitic absorption (Lemercier et al. 2020).

A challenge in fabricating planar PIN PSCs on a flat TCO electrode is to obtain a smooth, pinhole-free perovskite film to avoid leakage current by the one-step spin-coating method. There were more pinholes in the case of the PIN architecture when compared to NIP (Lemercier et al. 2020). The presence of a mesoporous scaffold facilitates conformal, continuous coverage of the absorber that fills its pores (Song et al. 2015) and can solve this.

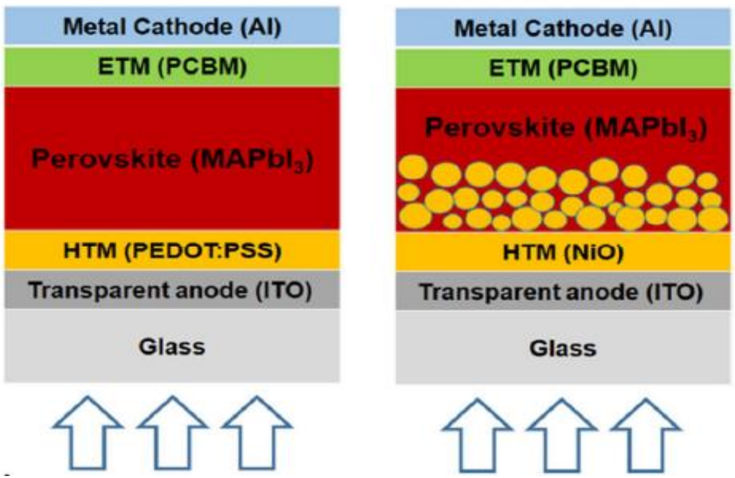

Figure 2 Left: PIN architecture perovskite solar cell; Right: Mesoscopic PIN perovskite solar cell. (Hussain et al. 2018)

The performances depend essentially on the chosen materials used as active and interfacial layers. The main weakness of these architectures can be the lower value of V_{oc}, due to the use of non-suitable n- and p-type interfacial layers. This prevents the optimal operation of the perovskite layer and favours the radiative recombination (Luo et al. 2018).

Dagar et al. recorded that devices maintained about 80% of the initial average PCE during maximum power point (MPP) tracking for >700 h for a PIN PSC with a PCE of 19.4% for a 2.2 cm^2 active area (Dagar et al. 2021). A robust device architecture and reproducible deposition methods are

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fundamental for high performance and stable large-area single junction and tandem modules based on PSCs.

2.2. NEGATIVE-INTRINSIC-POSITIVE (NIP)

The NIP architecture PSCs have led to the published record efficiencies for single-junction cells, 25.7% (Min et al. 2021). Such an architecture comprises a compact electron transporting/ selective layer (ETM/ETL) onto which the perovskite layer is deposited. Typically shows higher efficiencies compared to PIN-type PSCs using similar perovskites, as PIN architecture shows lower open-circuit voltage (Voc) for the non-suitable doping state of the perovskite near its N-type interface leading to a higher non-radiative recombination rate (Lemercier et al. 2020).

The NIP architecture also reported lower pinhole production during fabrication which resulted lower leakage of current (Lemercier et al. 2020).

In an NIP architecture, the stability of the HTL becomes important because of its contact with humidity and oxygen. NIP PSCs based on Cu_2O nanocubes HTMs achieved an efficiency exceeding 17% shows high stability (Elseman et al. 2019).

The efficiency of such architecture is slowly approaching the 25.5% for the mesoscopic-NIP architecture (Lekesi et al. 2022). Min et al. recorded that devices maintained about 90% of the initial average PCE during maximum power point (MPP) tracking for >500 h for a NIP PSC (Min et al. 2021).

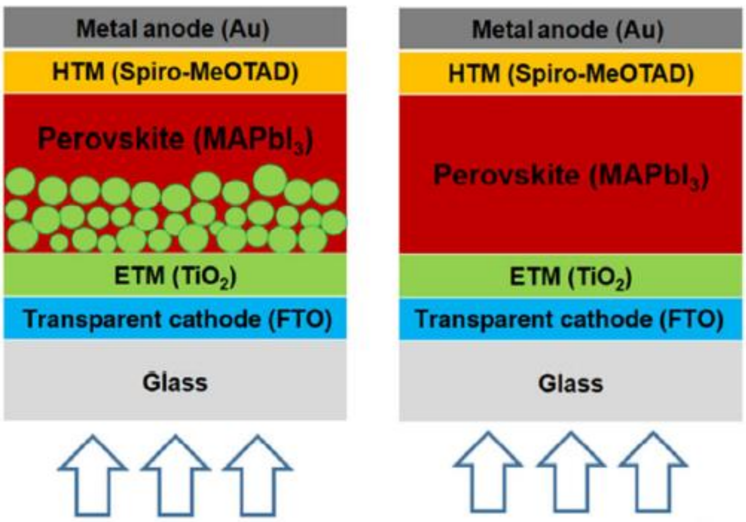

Figure 3 Left: Mesoscopic NIP perovskite solar cell; Right: NIP architecture perovskite solar cell (Hussain et al. 2018).

Although the NIP architecture demonstrates high efficiencies, their stability still suffers due to the negative impacts (e.g., degradation) imposed on the perovskite layer by the acidic and hydrophilic nature of the traditional Spiro-MeOTAD and PEDOT:PSS HTMs (Lekesi et al. 2022). Like the PIN architecture, the performances depend essentially on the chosen materials used as active and

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interfacial layers. When a thick less reactive insulating oxide layer (ZrO_2, ≈2 µm) is employed on top of TiO_2, the PSCs showed one of the highest stability (1000 h under light soaking) (Mei et al. 2014).

2.3. MECHANICALLY STACKED FOUR-TERMINAL (4T) DEVICE

4T tandem device, the third key device architecture for this work package, records a theoretical efficiency limit up to 43% (Lemercier et al. 2020). Such an architecture can be fabricated and optimized independently. Consequently, the device performance is not constrained by current-matching, and the tandem efficiency is simply the sum of each sub cell.

4T tandem devices with high efficiencies are typically fabricated on indium tin oxide (ITO)/glass substrates, with a multi-layered electron-transport layer (ETL), perovskite absorber layer, hole-transport layer (HTL), buffer layer, and ITO top contact. The mechanically stacked four-terminal tandems have currently achieved a PCE of 29.2% for perovskite–Si tandem (Emiliano Bellini 2021). Three transparent electrodes are required for 4T architectures, which could lead to higher parasitic absorption and manufacturing cost, as well as lower practical efficiencies (Hu et al. 2019).

Study on bifacial 4T perovskite silicon tandem module in outdoor condition (study on 100 h) showed promising performance (power density 20% higher) while comparing to the monofacial device (Coletti et al. 2020).

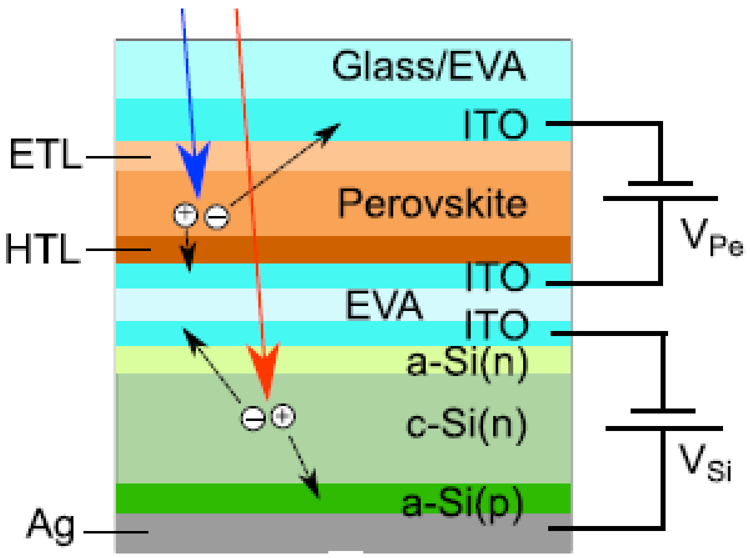

Figure 4 4-terminal tandem architecture (Gota et al. 2020).

2.4. MONOLITHIC TWO-TERMINAL (2T) TANDEM

Recent advances in device processing enabled the 2T architecture with optical advantages that have enabled the highest PCE for perovskite/c-Si tandems, 29.8% HZB 2021). In a monolithic 2T tandem,

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the two sub cells are electrically connected through a recombination layer or tunnel junction. As a result, only one transparent electrode is required, which allows the device to be more easily integrated into a photovoltaic system.

The current records for two-terminal devices are 29.8 % for a perovskite–silicon tandem HZB 2021), 26.4% for a perovskite–perovskite tandem (Lin et al. 2022) and 24.2% for a perovskite–CIGS tandem (Jost et al. 2020 - 2020).

Tandem cells of this architecture have the merits of simple electrical connection, lower manufacturing cost, minimized parasitic absorption and higher efficiency potential. A tandem cell with high efficiency should therefore have minimized undesirable absorptions, especially from the illuminated tandem's side. (Lemercier et al. 2020)

However, it also poses strict process compatibility and great challenges: 1) processing of the top-cells without damage to the temperature-sensitive bottom devices; 2) current-matching between the two subcells for minimal power loss with use of appropriate recombination layers, since the overall current output is limited by the lower one; 3) optical management within the tandems due to their sensitivity to spectral variations in time or geographical location, which may impact the energy yield (Hu et al. 2019).

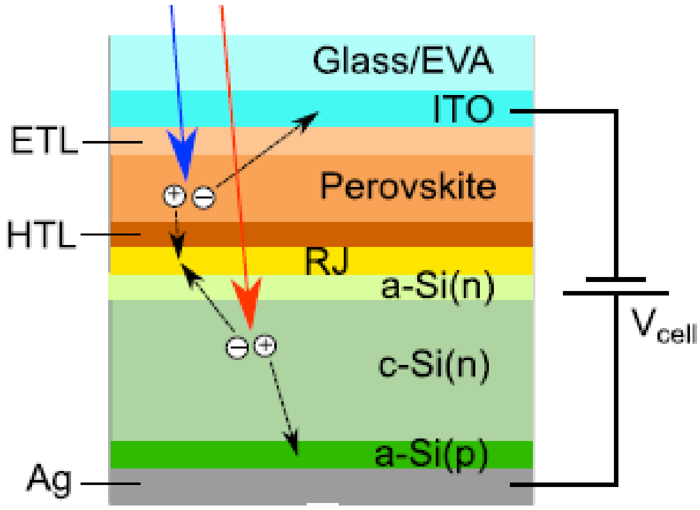

Figure 5 2-terminal tandem architecture (Gota et al. 2020).

For both 4T and 2T tandem Dupre et al. has established that even if defect-free, absorber layers suffer from both Auger and radiative recombination (Dupré et al. 2018).

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3. LAYER WISE MATERIAL LIST FOR KEY DEVICE ARCHITECTURES

This section details the individual materials used for the different layers within the perovskite SJ and tandem architectures described previously. The material list for the key device architectures is comprised of materials commonly used in labs and industries. The decision for which materials are selected is based on the feedback of the project consortium members based on their experience and current usage in literature. The materials thus signify the most common and promising candidates for each layer of the device architectures.

In order to refine the material list, it is also decided to employ certain evaluation criteria to each of the individual materials over the course of the project. The following are considered as evaluation criteria:

- Technology Readiness Level (TRL) of processing technology – The TRL provides the maturity of a technology going from TRL1 (basic principles observed) to TRL 4 (technology validated in the lab) to TRL 9 (actual system proven in operational environment). Moving over the TRL scale allows one to confirm reproducibility, repeatability, reusability, stability over time and the up-scalability of the evaluated technology (European Commission. Directorate General for Research and Innovation. 2017). Processability & scalability of the processing technology in relation to the materials processed is considered under the TRL.
- Material toxicity – higher the calculated toxicity, greater is the impact on the environmental profile of the technology such as eco-toxicity, human toxicity and eutrophication.
- Material criticality – corresponds to material availability and whether sufficient amounts of material are available, specifically relating to TW scale production of photovoltaics in the coming years.
- Device Stability – corresponds to the lifetime of the device, based on the individual layer stacks within. Higher the device stability, lower is the impact on the environment and the costs.
- Device Performance – corresponds to the efficiency and/or power output of the device, based on the individual layer stacks within. Higher the device performance, lower is the impact on the environment and the costs.
- Price – corresponds to the price of the individual materials within the device. Price of the individual materials directly influences the production cost of the device and subsequently the LCOE. Higher the price, higher the production cost. It is to note, that current low volume prices of materials may reduce significantly with industrialization owing to economies of scale.

It is important to note that the above criteria will need to be evaluated concurrently for each material/device. For example, a low price for a material may provide lower production costs but may also have poor stability which would increase both the environmental impact as well as the LCOE and vice versa.

Table 1 below shows considered materials for the key device architectures. Within the list, the material and architecture denoted “y” are considered yes while “(y)” represented feasible, but not demonstrated in high efficiency.

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Table 1 List of materials selected for the key device architectures within the VIPERLAB project.

Layer	Materials (add all relevant materials)	Processing technology		PIN	NIP	2T		4T	
		1st step	2nd step			PIN	NIP	PIN	NIP
HTL (PIN) / ETL (NIP)	NiOx	PVD		y		y		y	
	PTAA	Printing, spin coating		y		y		y	
	SAM (2PACz, MEO2PACz, ME4PACz, …)	Wet chemical (spin coating/blade coating)		y		y		y	
	P3HT: Poly(3-hexylthiophene-2,5-diyl)	Slot-die		y					
	Bifluo-OMeTAD	Slot-die		y					
	Spiro-OMeTAD	Spin coating		y					
	SnO2	CBD			y				
	TiO2	e-beam evap.			y		y		
	PEDOT:PSS	Blade Coating, Slot die (with isopropanol)		y	y	y	y	y	
Absorber	Generic ABX3 with B=Pb, A and X variable	single solution spincoat		y	y	y	y	y	y
		single solution blade coat		y	y	y	(y)	(y)	y
		single solution slot die		y	y	(y)	(y)	(y)	(y)
		single source evaporation		y	y	(y)	(y)	(y)	(y)
		co-evaporation		y	y	y	(y)	y	y
		CsX/PbY2 PVD	MAX/FAX CVD	y	y	(y)	(y)	(y)	(y)
		CsX/PbY2 PVD	MAX/FAX spincoating	y	y	y	y	y	y
		CsX/PbY2 PVD	MAX/FAX slot die	y	y	(y)	(y)	(y)	(y)
		CsX/PbY2 PVD	MAX/FAX blade coating	y	y	(y)	(y)	(y)	(y)
		generic Pb template by sputtering or PLD	RPI treatment	(y)	y	(y)	(y)	(y)	(y)

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Layer	Materials (add all relevant materials)	Processing technology	PIN	NIP	2T	4T
Interface buffer layer	LiF	Evaporation	y		y	y
	PMMA	solution processing	y	y		y
	other materials/molecules (name most important ones)					
ETL (PIN) / HTL (NIP)	C60	Evaporation	y		y	y
	PC61BM	Blade Coating (with chloroform)		y		
	Bis-C60	Blade Coating (with isopropanol)		y		
	PCBM	Printing, Wet chemical, (blade coating, slot die)	y	y	y	y
Buffer	ZnO	Slot die (with acetone) / PVD	y	y		
	BCP	PVD/solution	y		y	
	TiO2	Screen printing	y			
	SnOx	ALD / PVD	y		y	y
TCO	AZO	ALD, PVD	y		y	y
	ZrO2	Screen printing	y		y	
	ITO	Sputtering	y	y	y	y
	IZO	Sputtering	y	y	y	
	AZO	Sputtering or Wet chemical	y		y	
Electrode	Ag	Screen printing or evaporation	y	y		
	Ag	Dispensing				
	Carbon	Screen printing	y			
	Au	Evaporation	y			
	Cu	Plating / Evaporation	y			

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Layer	Materials (add all relevant materials)	Processing technology	PIN	NIP	2T		4T	
Substrate	Glass-FTO		y		y		y	
	Glass-ITO		y				y	
	PET-ITO		y	y				
	PET-FTO							
	PEN-ITO			y				
	PEN-FTO							
	PI		y				y	
	Flexible glass							
Tandem devices using Low bandgap perovskite cell (see below)								
Tandem bottom cell type	SHJ				y			
	CIGSe	PVD			y			
	TO-PERC				y			
HTL	PTAA	Blade Coating, Slot die						
	SAM (2PACz, MEO2PACz, ME4PACz, …)	Blade Coating, Slot die (with isopropanol)						
	PEDOT:PSS	Blade Coating, Slot die						
	NiOx	CDB, PLD,e-beam evap, hydrolysis						
Absorber	Generic ABX3 with B=Pb/Sn, A and X variable	single solution spincoat	y	y	y	y	y	y
		single solution blade coat	y	y				
		single source evaporation						
		co-evaporation	y	y				
		CsX/Pb/SnY2 PVD MAX/FAX spincoating	y		y			
ETL	C60	Evaporation	y		y	y	y	y
	PC61BM	Blade Coating (with chloroform)		y				
	Bis-C60	Blade Coating (with isopropanol)		y				

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	PCBM	Printing, Wet chemical, (blade coating, slot die)	y	y	y	y
Buffer etc. analog to SJ						

Layer	Materials (add all relevant materials)	Processing technology	PIN	NIP	2T	4T
Encapsulation	EVA		y			y
	POE		y			y
	UV resin		y			y
	3M		y			
Edge sealant	Butyl Rubber		y			

Furthermore, the material list is circulated to the advisory board consisting of leading industry players for validation and feedback on the following questions:
• Which materials are missing from the list? Which are not relevant and can be removed?
• Which evaluation criteria are missing from the list? Which are not relevant and can be removed?
• Qualitative rating of PIN vs NIP perovskite SJ device and 2T vs 4T tandem device - which device is the most promising in terms of entering the market?

Any feedback received on missing materials and evaluation criteria is included in this report. For the last question the advisory board believes that the four different key device architectures are in an open race with pros and cons for each technology. From the feedback, two-third preferred PIN architecture over NIP for the SJ perovskites since it is still unclear which production compatible layer is to be used as HTL for NIP. Tandems are preferred over SJ as SJ perovskite cannot complete with SJ silicon. Moreover, the feedback, in general, included the opinion that 2T tandem devices for power generation (Solar Panels) and flexible PIN for powering IoT devices (Solar mini-modules) can be a promising approach in terms of entering the market.

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4. SUMMARY AND NEXT STEPS

The deliverable report D10.1 within the VIPERLAB project addresses the first task related to the provision of data (material, process flows, etc.) required for carrying out an economic and environmental assessment. The project consortium has selected four key device architectures as described in section 2 and further provided a layer-wise list of materials that are commonly used (refer section 3). The selected architectures are:

i.) positive-intrinsic-negative (PIN),
ii.) negative-intrinsic-positive (NIP),
iii.) 2-Terminal (2T) and
iv.) 4-Terminal (4T).

The project consortium believes that these four different key device architectures are in an open race with pros and cons for each technology. Both the key device architectures and material list are sourced from the current usage in literature and the feedback of the project consortium members based on their experience and, therefore signifying the most common and promising candidates currently used in labs and industries. In addition, to ensure and validate the selection, certain evaluation criteria are also decided upon to be deployed concurrently for each material/device throughout the project. Thus, the material list aims to be a ‘living’ database with further refinement by implementing the evaluation criteria over the course of the project. It is important to note that the material list is also validated and reviewed by the advisory board consisting of leading industry players and their feedback, where available, is incorporated.

To address the second task of WP10 (), data on price, material consumption and processing equipment (parameters such as CAPEX, throughput, yield, etc.) for each material is required as a next step. This will enable the environmental Life Cycle Assessment social and economic Levelized Cost of Electricity impact assessment of the selected device architectures with the chosen materials. The results from such an assessment will contribute significantly to VIPERLAB’s overall goal to establish an EU-based perovskite PV production with the lowest costs and the lowest carbon footprint.

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